TCAD Based Analysis of Gate Leakage Current for High-k Gate Stack MOSFET

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***Abstract*— Scaling of metal-oxide-semiconductor transistors to smaller dimensions has been a key driving force in the IC industry. This work analysis the gate leakage current behavior of nano scale MOSFET based on TCAD simulation. The Sentaurus Simulator simulates the high-k gate stack structure of N-MOSFET for analysis purpose. The impact of interfacial oxide thickness on the gate tunneling current has been investigated as a function of gate voltages for a given equivalent oxide thickness (EOT) of 1.0 nm. It was reported in the results that interfacial oxide thickness plays an important role in reducing the gate leakage current. It is also observed that high-k stack gated MOSFET exhibits improved performance in term of Off current and DIBL**

***Index Terms*-MOESFET, inelastic trap assisted tunnelling, gate tunneling current, High-k stack**

I. Introduction

High-k gate stack structures as possible candidates to replace silicon dioxide layer for nanoscale MOSFETs have been of great interest very recently due to their promise in reduction of gate current in order to reduce standby power consumption of CMOS circuits. When the device feature sizes reach nanoscale dimensions, gate oxide thickness approaches its manufacturing and physically limiting value of less than 2 nm [1], leading to higher gate tunneling current. To reconcile the need for reduced gate leakage current in highly scaled devices, the replacement of SiO_2 as gate dielectric with alternate high-k dielectric material is considered as a method to contain/reduce the gate leakage current [2]-[6].Research on high-k dielectrics quickly converged on the Al_2O_3, HfO_2, and ZrO_2 family [7-11]. However, HfO_2 and ZrO_2 received most attention based on their better thermal stability with Si [12-13]. The main concern for high-ê dielectrics include several orders of magnitude more comparison with direct tunneling current and must be taken into account when calculating/modeling the gate current for traps found in the bulk or interface [13].Consequently, trap-assisted gate tunneling current cannot be neglected in nanoscale CMOS devices in modern simulators. In this work, stacked gate dielectrics are investigated with respect to gate tunneling current. The poly Si/high- k/SiO_2/Si stack gated MOSFET structure is designed in santaurus simulator which accounts for trap assisted tunneling mechanism. Here, three different high-k gate stack structure have been analyzed. The impact of introduction of high-k gate stack on DIBL, SS, on current and off current have also been reported. In Section II, energy band diagram of poly Si/high-k/SiO_2/Si stack gated MOSFET is established. The high-k gate stack device structure and design used for simulation set up is presented in Section III. The results obtained are discussed in Section IV. A conclusion is given in Section V.

II. High-k Gate Stack Energy Band Diagram of Nano MOSFET

The schematic energy band diagram of the tunneling mechanism in high-k MOSFET is shown in Fig. 1.

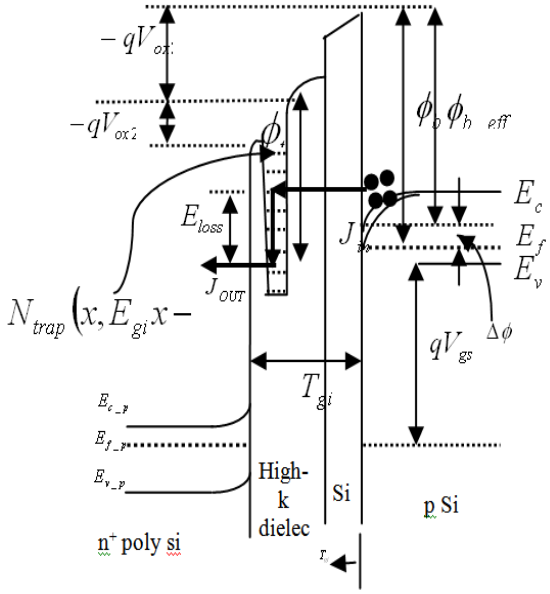

Fig. 1 Energy band diagram showing the two step inelastic trap assisted tunneling through stacked high-k gate dielectrics

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The Fig. 1 illustrate the energetic situation for a p-type Si substrate and a n^+- doped poly Si gate electrode.

One path is to tunnel directly through the top of energy band into the probe tip (J_{in}), and the other path is to tunnel via the isolated traps within the gate insulator (J_{out}). In the latter, electrons injected from the High-k/SiO_2/Si interface will ûrst tunnel to the nearer trap, then to the farther trap, and ûnally out of the gate insulator.

III. Simulation set up

Fig. 2. shows the schematic of device structure of N-MOSFET with high-k gate dielectric used in this study.

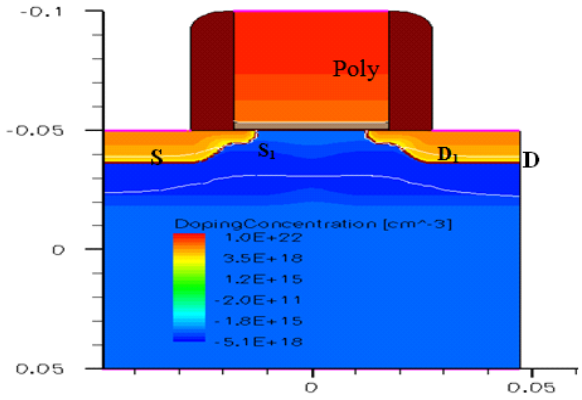

Fig. 2. NMOSFET device structure with stacked high-k gate dielectrics used in simulation

The deep S/D region is composed of a heavily doped silicon and a silicide contact. The doping of the silicon S/D region is assumed to be very high, $1x10^{20}$ cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 20 nm long and 50 nm high. This gives a large contact area resulting in a small contact resistance. The doping concentration of the acceptors in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of $1x10^{18}$ cm^{-3} and $1x10^{17}$ cm^{-3} near the channel. The halo implantation done around the S/D also reduces short-channel eûects, such as the punch-through current, DIBL, and threshold voltage roll-oû, for diûerent non-overlap lengths.

The MOSFET has a 50-nm-thick n+ poly-Si gate with metallurgical gate length of 25 nm and a 1.0 nm gate oxide. The doping concentration in polysilicon gate is $1x10^{22}$ cm^{-3} at the top and $1x10^{20}$ cm^{-3} at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and poly silicon. The oxide spacer has been assumed to reduce the gate capacitance. Here, Lo represents the overlap length, which is controlled by the S/D implantation energy. Lo = 5 nm optimized with off current is used in this work. The MOSFET with L_{met} of 25 nm was designed to have a V_T of 0.19 V. We determined V_T by using a linear extrapolation of the linear portion of the I_{DS}-V_{GS} curve at low drain voltages. The operating voltage for the devices is 1V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width.

MOSFET devices in nano regime are characterized by several aspects typical of the manometer scale: short channel eûects, quantum conûnement in the channel, tunnel current through the gate dielectric, source-to-drain tunnel current, inelastic scattering along the channel and far-from-equilibrium transport. From this point of view TCAD models [14] that are adequate to represent the device physics appropriately during simulation at nano regime are included. Comparison of some of these transport models can be found elsewhere [14].

Scattering inside the intrinsic device is treated by a simple Brooks–Herring model, which gives a phenomenological description of scattering. This simple model can capture the essential physics realistically. Enhanced Lombardi Model is used for mobility which accounts for the mobility degradation due to high-k gate dielectric [14]. Thus, the simulation of the device is performed by using Santaurus design suite [15] with drift-diûusion, density gradient quantum correction and advanced physical model being turned on.

Iv. Results and discussion

In this section, simulation of gate tunneling currents for a n-channel fully depleted nanoscale MOSFET through different stacked high-k dielectric structures have been carried out.

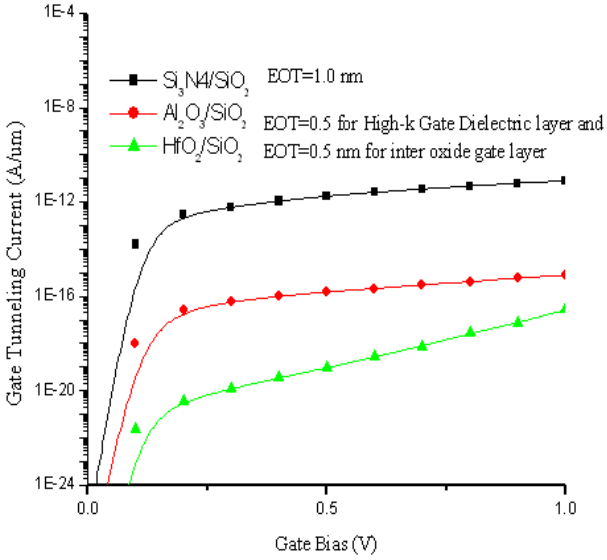

Fig 3. Santaurus simulated data for different gate stack viz: poly Si/Si_3N_4/SiO_2/Si, poly Si/Al_2O_3/SiO_2/Si and poly Si/HfO_2/SiO_2/Si with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

The variation of total gate tunneling current with gate bias for a given values of EOT has been presented for possible alternative stacked gate dielectrics such as poly Si/Si_3N_4/SiO_2/Si, poly Si/Al_2O_3/SiO_2/Si and poly Si/HfO_2/SiO_2/Si. The impact of inter layer dielectric thickness, type of gate stack and reverse gate stack on gate tunneling current as a function of gate voltages is reported in results for a given equivalent oxide thickness (EOT) of 1.0 nm with a 0.5 nm EOT for oxide and 0.5

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EOT for high-k gate dielectric. The impact of introduction of high-k gate stack on off current and DIBL have also been reported.

The simulated results for gate tunneling current through different gate stack such as poly Si/HfO_2/SiO_2/Si, poly Si/Al_2O_3/SiO_2/Si and poly Si/Si_3N_4/SiO_2/Si is presented in Fig.3.It is shown in Fig. 3 that gate tunneling current reduces with the increase in dielectric constant of the stack . This may be due to the fact that the possibility of carrier tunneling directly from channel to gate is low at large physical thickness of gate insulator (high-k gate dielectric) for a given equivalent oxide thickness (EOT) because physical thickness increases with dielectric constant.

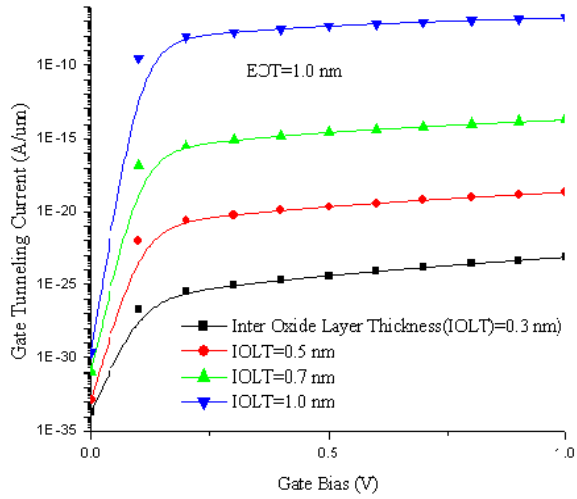

Fig 4. Gate tunneling current vs gate bias with inter layer thickness of oxide layer as a parameter poly Si/HfO_2/SiO_2/Si stack with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

The high-k gate stack structure consisiting of poly Si/HfO_2/SiO_2/Si is taken as an example to analyse the gate tunneling current behaviour with thickness of inter oxide layer for same EOT of 1.0 nm in this work. The gate tunneling current for different inter oxide layer thickness is illustrated in the Fig. 4 to show the effects of inter oxide layer thickness. In this case, the gate tunneling current is reduced with increasing thickness of the inter oxide layer for the same EOT. This may be due to the fact that decrease in inter oxide layer thickness translates to increases in physical thickness of high-k dielectric layer. This increased physical thickness of high-k , in turn, lowers the vertical field responsible for carrier tunneling and reduces the gate tunneling current. However, it is also noted that the effect of gate current reduction with inter oxide layer cannot be generalized since the magnitude of gate current in high-k stack structures with inter oxide layer also depends on the interplay between other factors such as the barrier height, electron effective masses, as well as dielectric constant of the individual layers.

Fig. 5 plots the gate tunneling current vs gate bias with and without inter oxide layer i.e. for individual HfO_2 gate dielectric and HfO_2/SiO_2 gate stack respectively at an EOT of 1.0 nm. It is observed that gate tunneling current reduces to large extent for high-k gate stack as compared to individual high-k gate dielectric for same EOT. This may be due to the large interface barrier encountered by the tunneling electron when oxide layer is incorporated between high-k layer and substrate Si

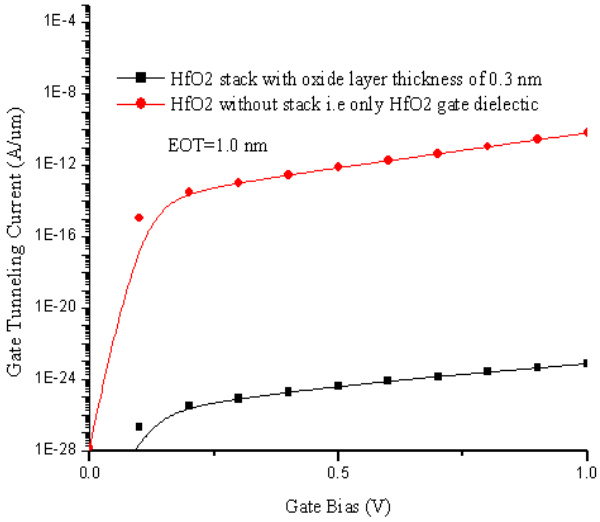

Fig.5. Gate tunneling current vs gate bias with and without oxide layer for HfO_2 gate dielectric at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

Another important issue is the effect of introduction of high-k gate stack structure on off current of the device. The off current improves for high-k gate stack structure in comparison to individual high-k gate dielectric as illustrated in Fig. 6. Since threshold voltage deceases with increase in fringing field coupling with channel carrier, so, introduction of high-k gate stack structure slightly increases the threshold voltage due to lower fringing field coupling with carrier. This , in turn, reduces the subthreshhold leakage thereby improving the off current of the device.

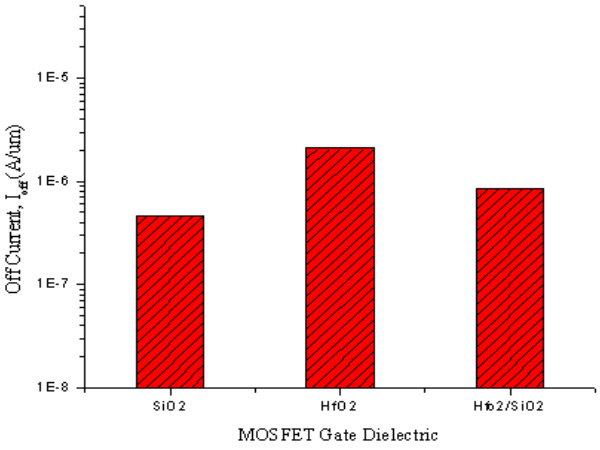

Fig.6. Off current vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/ SiO_2/HfO_2/Si gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

Fig. 7 represents the variation of DIBL(drain induced barrier lowering) with gate dielectric material of the device to show the effect of gate dielectric material on DIBL.

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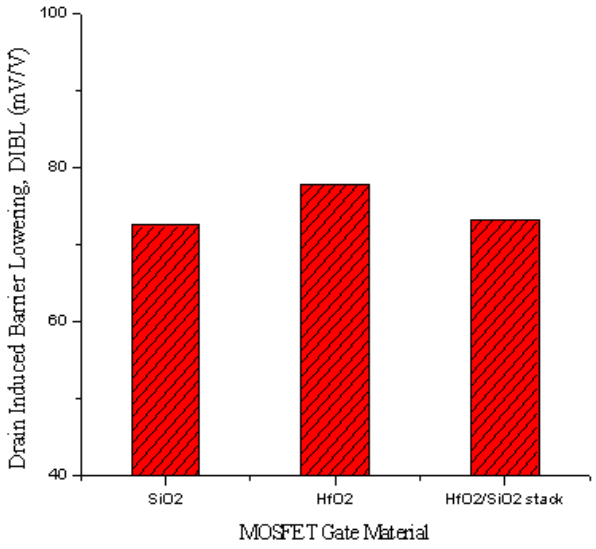

Fig.7. DIBL vs different gate dielectric such as only SiO_2, individual HfO_2 and poly Si/ SiO_2/HfO_2/Si gate stack at a equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

It is observed in Fig. 7 that DIBL improves marginally for high-k gate stack in comparison to individual high-k gate dielectric due to decreased effect of fringing field through high-k gate stack structure.

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IV.CONCLUSION

In summary, TCAD analysis of nano scale N-MOSFET having high-k gate stack structure such as poly Si/Si_3N_4/ SiO_2/Si, poly Si/Al_2O_3/SiO_2/Si and poly Si/HfO_2/SiO_2/Si has been performed. We have confirmed that the introduction of high-k gate stack MOSFET not only reduces the gate leakage current but also improves the other devices parameter as compared to individual high-k gate dielectric.

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